



Comparative Analysis of the Drain Current in a 7nm and 14nm Fully Depleted Silicon-On-Insulator (SOI) MOSFET

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ABSTRACT

This research investigates the influence of temperature on the drain current of a 7nm and 14nm Silicon-on-Insulator (SOI) MOSFET with Silicon (Si) and Gallium Arsenide (GaAs) as channel materials. The Semi-classical transport model is used to study the effect at 50K, 250K, 350K, 450K, 650K, and 850K. The 7nm and 14nm SOI MOSFET Si channels have low resistance when the temperature rises from 50K to 850K. Because the contraction in the channel size results in quicker injection of the electron with a high average electron velocity and high electron density, the drain current is virtually linear as the gate voltage increases. It was discovered that the drain current in the 7nm and 14nm GaAs SOI MOSFET channels is increased by an increase in mobility as the channel length reduces to the nanoscale dimension, with a decrease in resistance as the temperature rises. In the 7nm GaAs channel, the average electron velocity decreases as channel length increases at 50K, 250K, 350K, and 450K, then increases at higher temperatures of 650K and 850K, whereas in the 14nm GaAs channel, the average electron velocity increases as channel length increases at 350K, 450K, 650K, and 850K, then decreases at 50K and 250K. The results reveal that GaAs has greater electron mobility and a higher on-state current in both the 7nm and 14nm channels.

Keywords: Drain current, SOI-MOSFET, Gate Voltage, Channel Length, Temperature

1. INTRODUCTION

The silicon on insulator (SOI) Metal Oxide Semiconductor Field-effect Transistor (MOSFET) is a revolutionary technology that have been widely researched in order to develop high performance digital integrated circuits with low power consumption, high radiation tolerance, better scalability, decrease in short-channel effects, lower voltage and high-speed application (Neha and Manoj, 2016; Asmaa, 2013; Naveenbalaji and Viranjay, 2022). The advantage of constructing SOI MOSFET is that they solve various drawbacks inherent in the bulk silicon MOSFET such as minimal dimension in scaling, high drain/source parasitic capacitances, declining return in switching performance, significant resilience on process changes, off-state leakage current (Thomas, et al., 2003; Cristoloveanu and Li, 1999; Neha and Manoj, 2016; Gana, Galadanci, Darma and Tijjani, 2021). According to a 2009 assessment by the International Technology Roadmap for Semiconductors (ITRS), research and development for reaching a modified SOI structure with a device size of less than 16nm will continue until 2024 (Kuma, Vashishath, Gupta and Rashmi, 2022).

The SOI MOSFET structure consist of a thin body region of a single crystalline silicon layer separated from its bulk substrate by a thin insulating layer; the technology of this design is based on the use of a buried oxide layer of silicon dioxide (SiO₂) as the insulating layer and Silicon wafer as the substrate material (Mäkinen and Suni, 2020; Oleg and Bich-Yen, 2014). The SOI MOSFET is classified according to the film thickness of the SOI layer, which determines whether the device is fully depleted (FD) or partially depleted (PD) of majority carriers (Maddah, Bolouki, Afzali-Kusha and El-Nokali, 2002). The film thickness of partially depleted SOI MOSFET is thicker than the maximum depletion width of the gate, so that the channel (Doped channel) is partially depleted of majority carriers during operation, whereas the SOI film thickness of a fully depleted SOI MOSFET



is kept smaller than the depletion width of the gate, so that the channel (Lightly doped) is completely depleted of majority carriers during operation (Neha and Manoj, 2016; Collinge, 2008; Neha and Ankit, 2012).

Several studies have been conducted to investigate the influence of temperature on the drain current of an SOI MOSFET. (Jean-Pierre et al., 2008) presented a temperature study on a tri-gate SOI MOSFET measured between 5K and 400K of temperature, and reported that fully depleted SOI MOSFET operating at a temperature above 150K does not suffer from premature corner inversion, and electron mobility is limited by phonon interaction above 100K. However, surface roughness limits device functioning below 100K, and due to doping concentration, the corner film thickness (SiO₂) has a lower threshold than the Sidewall SiO₂ interface below 150K. (Neha and Ankit, 2012) investigated the effect of temperature ranging from 77K to 400K on the threshold voltage and mobility for partially depleted SOI MOSFETs and reported that in SOI MOSFETs with longer channel length, the doping concentration always limits the mobility of the electrons due to phonon interaction and also reaches full depletion at high temperature as compared to short channel length. At low temperatures, shorter channel lengths enhance mobility and threshold voltage. According to research on the drain current of fully depleted SOI MOSFETs with lightly doped N- underneath the N+ source area, the analytical model of a 2-D fully depleted SOI MOSFET in terms of surface potential, threshold voltage, and drain current gives superior electrical properties in terms of reduced OFF-state current and improved ON-state to OFF-state current (ION/IOFF) ratio (Vimal, Sunil, Nilesh and Chauhan, 2021).

There was no mention of the effect of temperature above 500K on an SOI MOSFET device with a change in channel material in the literature that was analyzed during the investigation (especially for compound semiconductive material). The literature concentrates on the electrical properties of the devices and ignores electron transport when the channel dimension is lowered to the nanoscale region. According to the new ohms law, when the channel dimension is reduced to the nanoscale region, the mean free path accounts for resistance given by electron drifting from the source to the drain such that the resistance does not approach zero. This study takes into account transport characteristics such as electron velocity and channel resistance as the channel shrinks to the nano region. Also, because changes in channel materials tend to improve electron mobility, this research focuses on a comparative examination of the influence of temperature on the Drain Current in the sub-micro-region of a 7nm and 14nm Silicon-on-Insulator (SOI) MOSFET with elemental semiconductor (Si) and binary compound semiconductor (GaAs) channel material using the semi-classical model as the physical channel length of the SOI MOSFET is modified correspondingly spanning a range of temperatures (50K, 250K, 350K, 450K, 650K and 850K).

2. THEORETICAL BACKGROUND

The unidirectional thermal velocity is critical in electron transport. The thermal average velocity of electrons with positive velocities is zero in equilibrium (Lundstrom and Ren, 2002; Ooi and Lim, 2016). The Maxwell Boltzmann statistics are assumed below the threshold and the thermal velocity (v_T) is provided by the equation;

$$v_T = \sqrt{2k_B T / \pi m^*} \tag{1}$$

Under equilibrium the effective mass is m^* , and the uni-directional thermal velocity is the average carrier velocity at the beginning of the channel (Lundstrom and Ren, 2002; Yee and Lim, 2015). The threshold voltage (V_T) is determined in the linear region for a lower value of V_{DS} by the different values of the gate voltage observed for the drain currents by (Shroder, 1998; Gana, et al., 2021; Lucovsky and Misra, 2001). Then the drain current may be calculated as;

$$I_D = \frac{\mu C_{ox} W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \tag{2}$$



where V_T is the threshold voltage, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, μ is the carrier mobility, C_{ox} is the oxide capacitance, W is the channel width, and L is the channel length. The gate oxide capacitance per unit area (C_{ox}) of MOSFET can be calculated using the equation (Nirmal, Kumar, and Jabaraj, 2010);

$$C_{ox} = \frac{\epsilon \times 2}{T_{ox}} \quad (3)$$

where T_{ox} is the oxide thickness and ϵ is the permittivity of the dielectric material. For an $I_{DS} - V_{GS}$, the equation results in a straight-line plot with an x -intercept given by (Shroder, 1998; Lucovsky and Misra, 2001);

$$V_{TE} = V_T + \frac{V_{DS}}{2} \quad (4)$$

At low drain current (for negligible resistance) the threshold voltage can be calculated by;

$$V_T = V_{TE} - \frac{V_{DS}}{2} \quad (5)$$

The current of a typical MOSFET (Drain Current) in the saturation region under high drain voltage is given by (Lucovsky and Misra, 2001);

$$I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 \quad (6)$$

The sub-threshold slope is important because it describes the measure of voltage swing needed to switch the MOSFET from its initial OFF to ON state, particularly for modern MOSFETs with supply voltages close to 1.0V (Muls, DeClerck, & Van-Overstraeten, 1978; Colinge et al., 2006). Under these conditions, the drain current of a MOSFET can be estimated using the equation;

$$I_D = I_{D1} \exp\left(\frac{q(V_{GS} - V_T)}{nkT}\right) \times (1 - \exp\left(\frac{-q(V_{DS})}{kT}\right)) \quad (7)$$

The constant current I_{D1} is always dependent upon the device temperature, dimensions, and substrate doping density of the device, the dimensionless quantity n is govern by the equation (Lucovsky and Misra, 2001);

$$n = 1 + \frac{C_b + C_{it}}{C_{ox}} \quad (8)$$

where C_b represent the depletion capacitance and, C_{it} represent the interface state capacitance. To acquire qualitative information about the interface state density the parameter n is always increases as the interface trap density and the doping density rise. The equation is proportionate to the charge which is an image of depletion charge and/or interfaces charge (placed on the gate) that does not result in an inversion of charge (Ooi and Lim, 2016);. The resistance R_{Load} of nano-MOSFET at the quasi-ballistic limit can be calculated by;

$$R_{load} = \left(\frac{V_{DS}}{I_{DS}}\right) = \frac{V_{th}}{I_{on-state at linear region} \times W} \quad (9)$$

3. METHODOLOGY

Nano-MOS for 2-D simulator for thin body devices is utilized in this work. The I-V data is derived from the source code (Wang, 2010). The elemental and compound semiconductors (*Si and GaAs*) are employed as channel materials. The Silicon channel thickness (T_{Si}) is fixed at 3nm, with a Top/bottom oxide insulator thickness (T_{OX}) of 1nm. The top and bottom dielectric materials are SiO_2 with Source/Drain doping concentration (ND) of $1.00E+18/cm^3$ and a constant Channel body acceptor impurity concentration (NA) of $1.00E+12/cm^3$. The

Gate/Source (VGS) and Drain/Source VDS) voltages are changed from 0.50V to 1.50V in 0.10V step. The Top and Bottom Relative Dielectric constant were both 3.9 respectively and the body Relative Dielectric constant was 11.7.

The semi-classical transport model is used to calculate the drain current and voltage for 7nm channel 14nm SOI MOSFET with a step size of 1nm from 00nm and operating temperature of 50K, 250K, 350K, 450K, 650K and 850K. The temperature variation simulation is performed by selecting the device type, transport model for the device geometry (ballistic transport using a semiclassical approach) and the input bias parameter. After entering the device description parameters and simulation options (vertical and horizontal node spacing, convergence parameters, and number of subbands) the program is run to acquire results.

4. RESULTS AND DISCUSSION

To obtain and validate the drain current of the SOI MOSFET in nanoscale of $L = 7\text{nm}$ and that of $L = 14\text{nm}$ for Si and GaAs channel materials the semi-classical model is employed. It was observed from Figure 1 of the 7nm and Figure 2 of 14nm Si channel SOI MOSFET that the drain current increases with an increase in temperature as the gate voltage increases from 1.0V with a step of 0.1V for both the low, average and high temperatures (50K, 250K, 350K, 450K, 650K and 850K). This is because the resistance decreases as temperature increases to overcome the barrier potential as shown in Figures 3, and Figure 4 and an increase in the gate voltage increases the drain current. This is because the barrier potential is being suppressed by high temperature and the resistance decrease with an increase in temperature allowing more electrons to flow from the source terminal to the drain terminal along the channel region. In the 7nm channel, the drain current is almost linear as the gate voltage increases because as the channel shrinks the electrons from the sources to the drain are injected faster with little resistance and the MOSFET will start behaving similarly to a simple wire obeying the conventional Ohms law. Considering the new ohms law that even with shrinkage of the channel dimension the mean free path will not allow the resistance to approach zero the electron can move freely drifting from the source terminal to the drain terminal along the channel region.

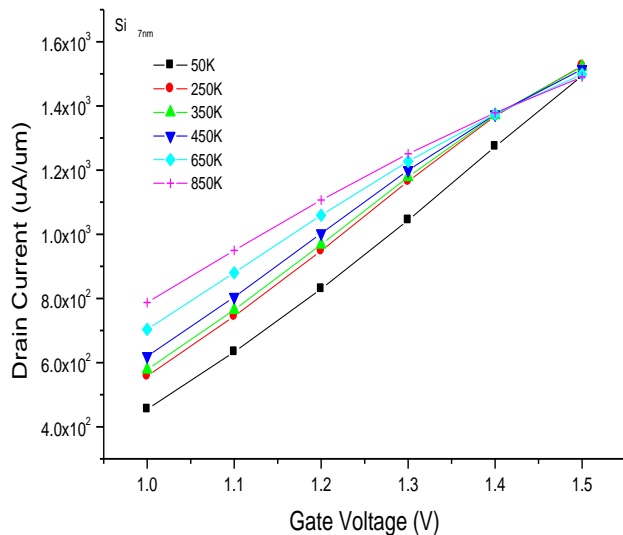


Figure 1: Drain current of 7nm Si channel

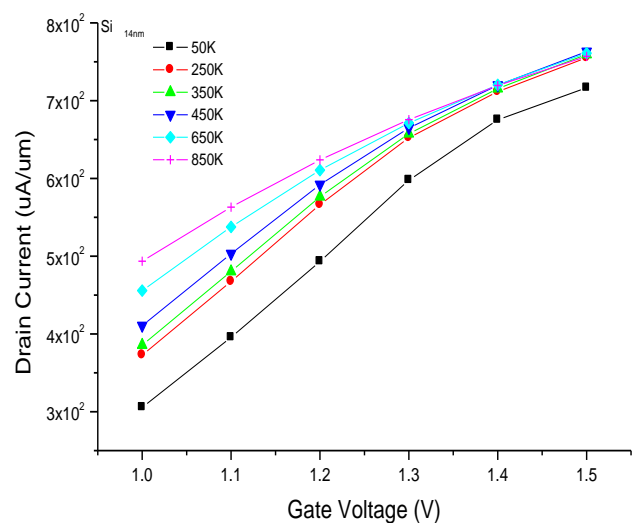


Figure 2: Drain current of 14nm Si channel

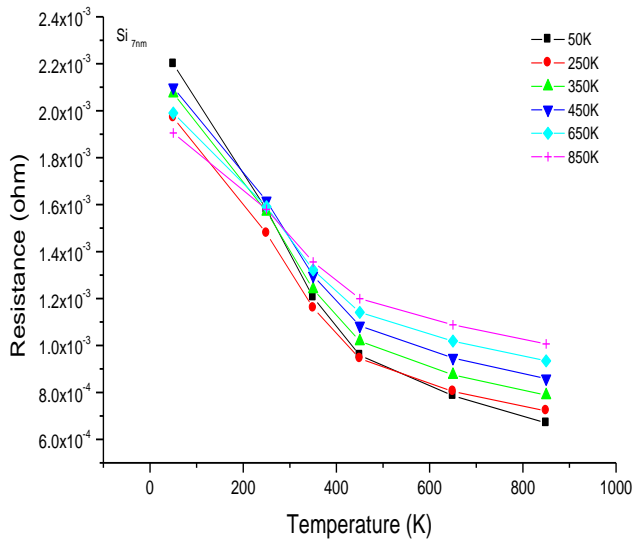


Figure 3: Resistance in 7nm Si channel

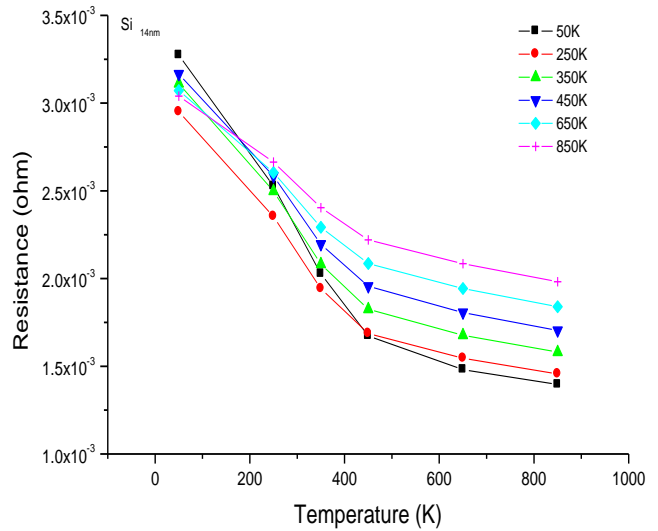


Figure 4: Resistance in 14nm Si channel

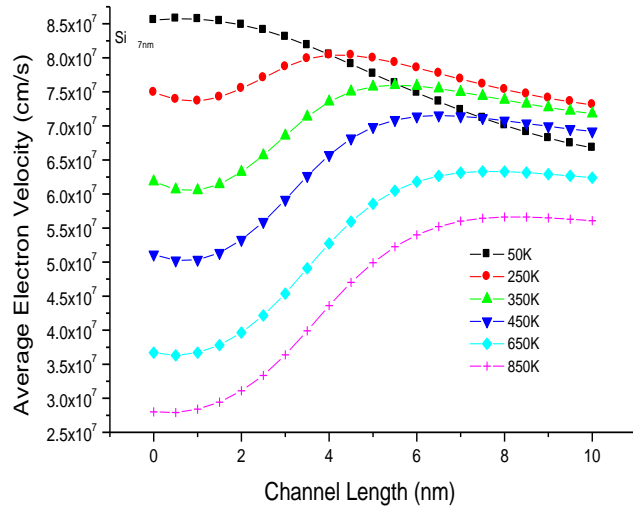


Figure 5: Electron Velocity in 7nm Si

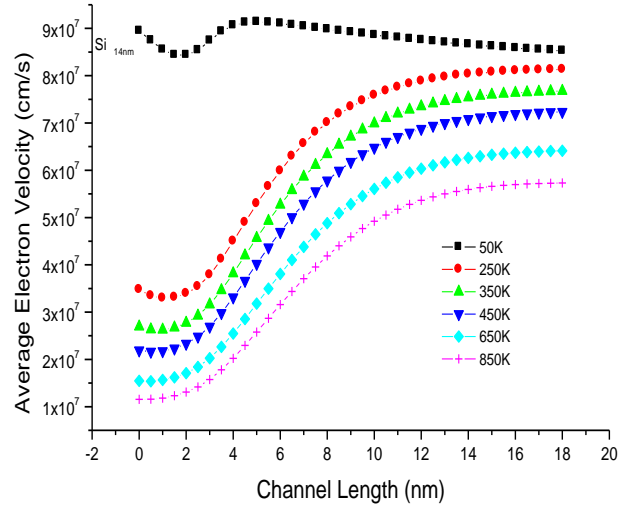


Figure 6: Electron Velocity in 14nm Si

At a very low temperature (50K) the average electron velocity is highest and decreases as the channel length increase. This is because, at low temperature, the barrier potential is very high causing high resistance and thus fewer electrons are free through the channel region near the source terminal. The drain current of the 7nm and 14nm GaAs is shown in Figure 7 and Figure 8 respectively. The drain current is always enhanced by the increase in mobility as observed in compound semiconductors as the channel length shrinks to the nanoscale dimension as such the behaviour is similar to that of the Si channel SOI MOSFET.

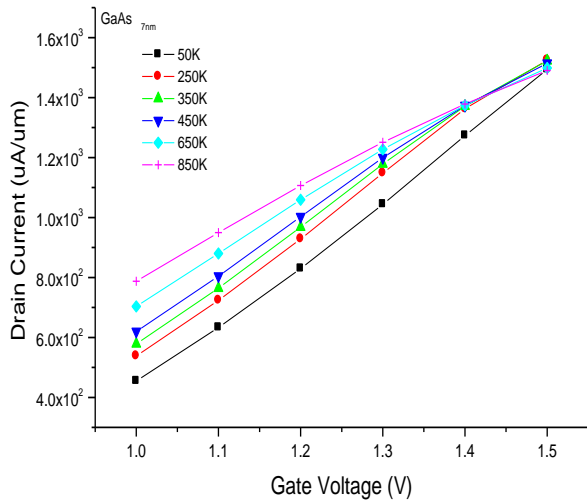


Figure 7: Drain current of 7nm GaAs

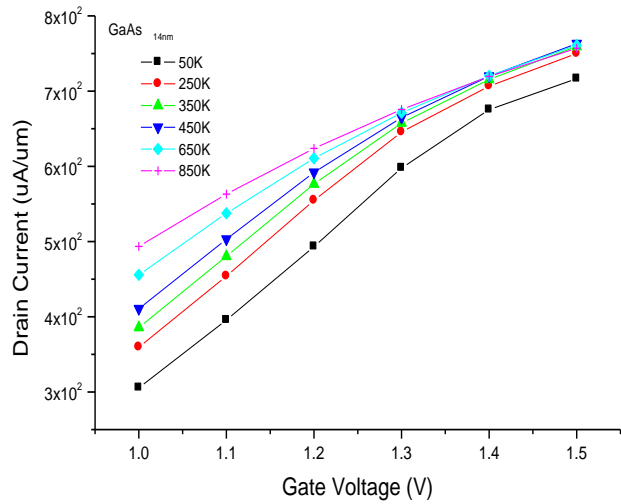


Figure 8: Drain current of 14nm GaAs

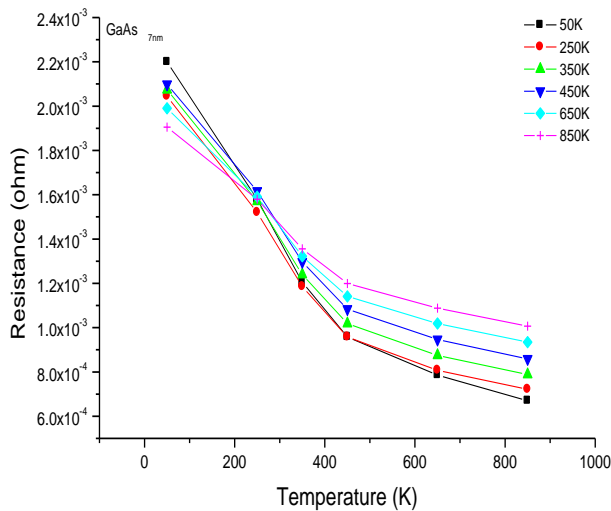


Figure 9: Resistance in 7nm GaAs

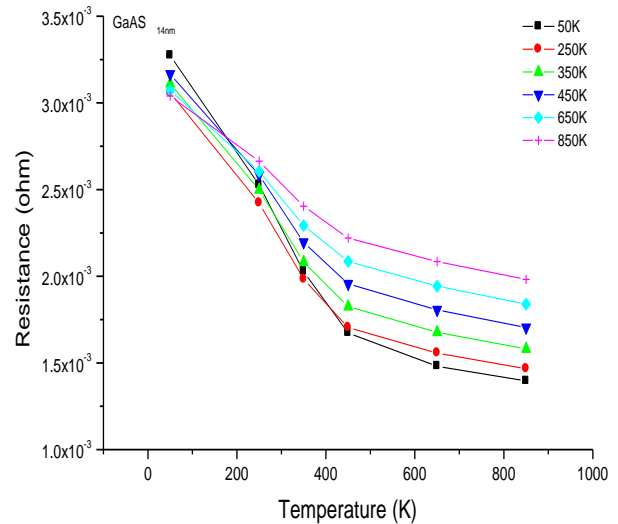


Figure 10: Resistance in 14nm GaAs

The resistance reduces with increasing temperature in the GaAs channel for both the 7nm and 14nm GaAs channels, as illustrated in Figures 9 and 10, respectively. This produces an on-state current (I_{on}), which is determined by the rate at which electrons are transported from the drain terminal (high electric field) zone to the source terminal (low electric field).

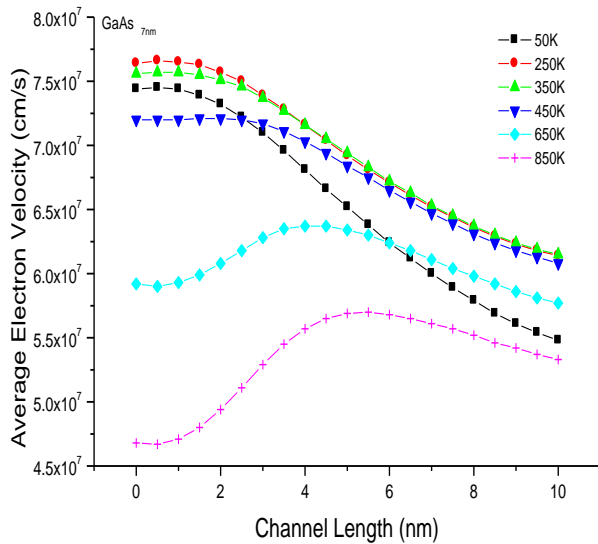


Figure 11: Electron Velocity in 7nm GaAs

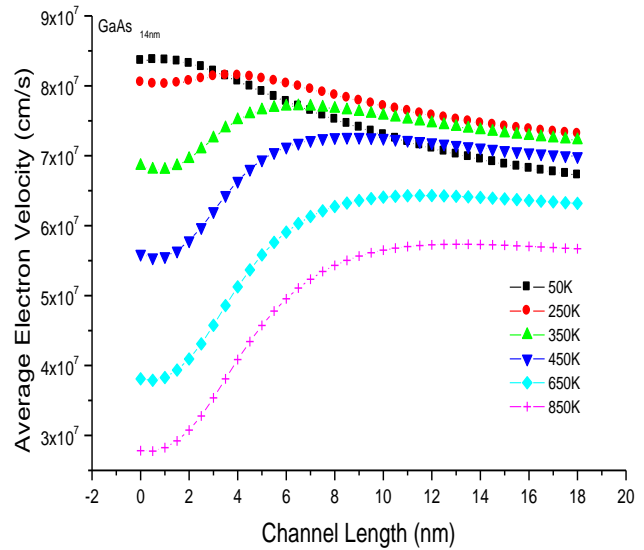


Figure 12: Electron Velocity in 14nm GaAs

The average electron velocity of a 7nm GaAs channel drops as the channel length grows at temperatures of 50K, 250K, 350K, and 450K, then increases at higher temperatures of 650k and 850k. The average electron velocity in the 14nm GaAs channel increases as the channel length increases at 350K, 450K, 650K, and 850K, then falls as the length increases at 50K and 250K with an increase in the gate voltage above $V_{GS} = 1.0v$. Because compound semiconductor channels (GaAs) have substantially better electron mobility than single compound semiconductor channels, the average electron velocity of the 7nm and 14nm GaAs is higher than the Si channel SOI MOSFET (Si). This indicates that the GaAs channel SOI MOSFET has improved electron mobility and, as a result, a faster on-state current (I_{on}).

5. CONCLUSION

The influence of temperature on the drain current of 7nm and 14nm SOI MOSFETs is explored in this study for elemental (Si) and binary compound (GaAs and InAs) semiconductors as channel materials using the semi-classical transport model at temperatures of 50K, 250K, 350K, 450K, 650K, and 850K using NanoMOS software. The results indicated that the drain current in the 7nm and 14nm SOI MOSFET Si channel is practically linear as the gate voltage increases and offers low resistance when temperature increases from 50K to 850K. GaAs provides better electron mobility with a high on-state current for both 7nm and 14nm channels, such that the average velocity of electron velocity in the 7nm GaAs channel decreases as the channel dimension changes (increase in length) from 50K, 250K, 350K, to 450K. At higher temperatures of 650K and 850K, the electron velocity (average velocity of electron) increases with an increase in channel dimension (change in length); whereas in the 14nm GaAs channel, the velocity of the electron increases rapidly with increasing channel dimension at 350K, 450K, 650K, and 850K, then decreases as the length increases at 50K and 250K.



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